

High efficient DC-AC inverter for low wireless power transfer applications

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ABSTRACT

The inverter's simplicity is an important aspect that must be considered, especially for electronic devices, as adding the number of power switches increases the complexity and overall cost of the inverter. This work proposes an inverter design that converts DC into AC power. It receives 12 VDC as an input voltage, and it is composed of a boost converter that converts an input voltage of 5–20 VDC to an output voltage of 4–30 VDC and a pulse width modulation controller to produce a square wave with a frequency of 100 kHz to drive the switching MOSFET. The designed inverter can be operated on different loads ranging from 50 Ω to 1000 Ω , tested in both simulations and experimentally. The design was optimized by the LT Spice simulator. The proposed inverter has operating frequencies ranging from 40 kHz to 110 kHz, taking into account different loads. The obtained results showed that both simulation and experimental results converged, whereas the highest efficiency was 96.96% at 55 kHz at a fixed load of 100 Ω . On the other hand, the maximum achieved efficiency when the load was sweeping was 80% at a load of 50 Ω at a fixed frequency of 100 kHz.

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1. INTRODUCTION

Wireless power transfer (WPT) technology has become more and more popular in recent years since it provides a useful and efficient means of receiving electrical energy for both stationary and mobile devices [1]. Dynamic wireless power transfer (DWPT), which involves the continuous supply of electricity to a moving device or vehicle, is one particular area of WPT that has drawn a lot of interest [2]–[4]. There are several potential applications for this technology, including those in the industrial sector [5], mobile devices [6] as well as charging for electric cars [7]. The omnidirectional wireless power transfer (OWPT) system's efficiency optimization is always a significant barrier to its use [8], [9]. As the central component of the OWPT system, a coupler possessing a proper volume, smooth coupling capabilities, uniform magnetic field distribution, and low losses is essential for achieving steady and effective energy transfer [10].

Applications for inverters include battery storage, solar panels, electric vehicles, air conditioning, uninterruptible power supplies (UPS), and high-voltage DC power (HVDC) transmission lines [11]. Square-wave inverters, sinusoidal two-level pulse width modulation (PWM) inverters, and multilayer inverters are the three types of inverters [12]. The ongoing advancement of WPT has made power-generating techniques

more important in light of the recent drive for ecologically friendly energy sources and practices. The production of electronic semiconductors has advanced quickly, which has presented a number of difficulties for the high-performance design of power inverters [13]–[16]. An inverter is an electronic device that contains many power switches. It is possible to create AC power from DC input by providing these switches with the appropriate control pulses [17], [18].

An inverter is an electronic device that contains many power switches. It is possible to create AC power from DC input by providing these switches with the appropriate control pulses [17], [18]. High frequency (HF) is necessary for many advantages. The use of high frequency in WPT allows for more efficient and precise transfer of energy, as well as potentially reducing interference and allowing for smaller sizes of the components [19], [20]. When it comes to minimizing size and reducing losses, greater frequency is the preferable option [21]. It's important to keep in mind that the precise frequency chosen for WPT is determined by the particular application and system requirements, with other factors such as safety standards and legal regulations also playing a role. The HF inverter is a key element in any WPT system [22]. Recent progress in research and methods has facilitated the creation of smaller and more portable electronics [23]. Power electronics converters have become indispensable in contemporary electronic devices due to their vital roles, enhancing the functionality and appeal of these devices.

Increasingly compact and portable power electronics are needed as systems for WPT become increasingly commonplace in daily life [24]. The HF inverter is used for the WPT application in this project, with the PWM controller inverter being the chosen converter [25]. The use of a high frequency switching frequency reduces the size of circuit components, such as transmitting and receiving inductors or capacitors [26]. Because the PWM technique reduces electromagnetic interference (EMI) and switching pressure, it is used for switching because it is straightforward and effective. This paper presents an optimal 110 kHz inverter layout for WPT devices with the ability to work under a wide range of different loads from 50 Ω to 1000 Ω .

While various inverter topologies, such as full-bridge and multi-level inverters, offer superior harmonic performance, they often introduce significant complexity and cost, making them suboptimal for low-power, cost-sensitive WPT applications. Similarly, prior single-switch designs have often been limited to narrow load or frequency ranges. The primary contribution of this work is therefore not the introduction of a new topology, but rather the systematic design, optimization, and experimental validation of a simple, single-MOSFET inverter that achieves a unique balance of high efficiency (>96%), robust performance across an exceptionally wide load range (50 Ω to 1000 Ω), and tunable high-frequency operation (40-110 kHz). This paper demonstrates a practical and reproducible solution that directly addresses the trade-off between performance, complexity, and cost for emerging low-power WPT systems. The rest of the paper is organized as follows: i) Section 2 explains in detail the proposed working design from the viewpoint of simulation and experiment design; ii) The obtained results are discussed in section 3; and iii) Finally, the conclusion of this work is presented in section 4.

2. SIMULATION AND EXPERIMENTAL DESIGN

To design the adopted inverter, the LT spice simulator was used, as shown in Figure 1. The proposed inverter consisted of a DC source (20 DCV), which would be inverted into AC power, a PWM controller (LTC4444), and a switching circuit (the main element is the MOSFET). The PWM is responsible for generating the square wave with a specific frequency to drive the MOSFET transistor via the gate terminal. At the beginning, the working frequency of the simulation setup ranged from 40 kHz to 110 kHz, whereas the load resistor was fixed to be 100 Ω . After that, the frequency in both practical and simulation was fixed to be 100 kHz, and the change in the load resistance value was from 50 Ω to 1000 Ω .

2.1. Experimental setup

Experimentally, the proposed inverter consisted of three essential circuits. These components include a boost converter and a PWM controller designed for signal management. Furthermore, a switching circuit was integrated, which incorporates both a gate driver and MOSFET circuit to produce the final output.

2.1.1. Boost converter

The XL6009 module, a non-isolated step-up boost voltage converter with an adjustable output voltage and good efficiency, is the boost converter (BC) employed in this work and is depicted. It changes a 5–20 VDC input voltage to a 4–30 VDC output voltage. A resistor divider connected to the XL6009 feedback pin controls the output voltage. The output voltage can be determined using (1).

$$V_{\text{out}} = V_{\text{Ref}} \left(1 + \left(\frac{R_5}{R_4} \right) \right) \quad (1)$$

Where (V_{Ref}) is the reference voltage, (R_4) and (R_5) are the feedback resistors. The advantages of using BC over a conventional boost converter are increased efficiency and improved reliability. The losses in the switch, diode, and inductor all affect the boost converter's efficiency (η) can be determined using (2).

$$\eta = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \quad (2)$$

In order to minimize current ripple and assure continuous conduction mode (CCM) functioning, the inductor value is selected. It is possible to compute the inductor value using (3).

$$L = \frac{V_{in} \times (V_{out} - V_{in})}{\Delta I_L \times F_s \times V_{out}} \quad (3)$$

Where (ΔI_L) is the peak- to- peak inductor current ripple, (F_s) is the switching frequency. Therefore, the value of the inductor in a circle boost converter consists of an inductor of 470 mH, a capacitor of 220 μ F on the input side and 100 μ F on the output side, a potentiometer of 10 k Ω , and a MOSFET XL6009 When the voltage source is connected to the BC circuit, the current flows through the coil, converting some energy into magnetic energy. Subsequently, the current passes through the diode, ensuring the correct direction and leading to the charging of capacitor C6. The output capacitor lowers ripple in the output voltage by smoothing it out. The necessary capacitance can be determined using (4).

$$C_{out} = \frac{I_{out} \times D}{V_{ripple} \times F_s} \quad (4)$$

Where (I_{out}) the output is current, (V_{ripple}) is the acceptable ripple voltage on the output. The variable resistance R5 the voltage value can be adjusted through the middle end of the variable resistance, which is connected to a terminal called FB. FB is used to compare the output voltage value with the reference voltage value through terminal No. 5 in the IC XL6009, which is connected to a terminal (FB). When the reference voltage equals the output voltage, the error decreases, but the output voltage remains constant. The VCC output is connected to the driver circuit at the end of the capacitor, which is connected to the drain end of the MOSFET.

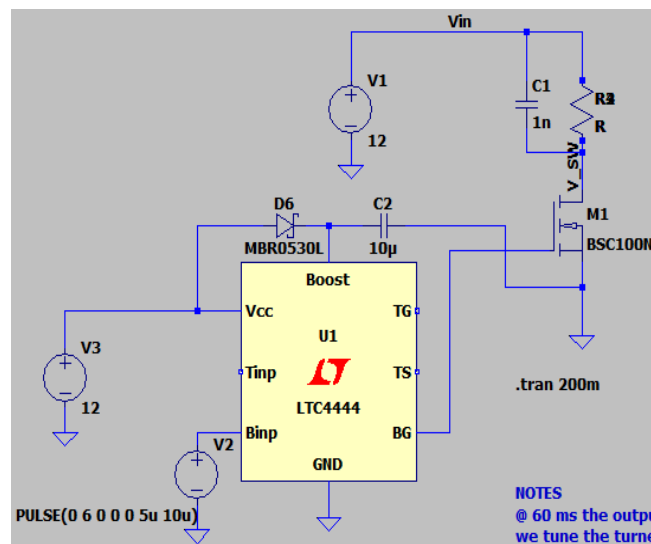


Figure 1. The simulated proposed inverter by the LT Spice platform

2.1.2. PWM controller design

A PWM controller based on the TL494 was developed, which is an adjustable multi-valued frequency pulse width modulation control circuit (from 40 kHz to 110 kHz). TL494's main characteristics are described as follows. Complete control circuitry for pulse width modulation, including an on-chip oscillator with master or slave operation, on-chip error amplifiers, an on-chip 5 V reference, adjustable dead-time control, and uncommitted output transistors with a 500-mA source or sink rating.

The block diagram of the TL494 output pulse width modulation, which is produced by comparing the capacitor's (CT) positive, saw tooth voltage with the other two control signal voltages. Transistors Q1 and Q2 can only be driven by the NOR gate when the flip-flop's clock input signal is low. The oscillator frequency is chosen by two components: the resistor (R_{RT}) and the capacitor (C_{CT}). The estimated oscillator frequency (F_{osc}) is determined by (5) [27].

$$f_{osc} = \frac{1.1}{R_{RT} \times C_{CT}} \quad (5)$$

Where (F_{osc}) the oscillator frequency in Hz is, (R_{rt}) is the timing resistor in ohm, (C_{CT}) is the timing capacitor in farads.

The voltage applied to the TL494's control input, as well as the reference voltage determine the PWM signal's duty cycle. The ratio of the PWM signal's on-time to its overall period is known as the duty cycle, or D. The duty cycle D can be expressed as (6).

$$D = \frac{t_{on}}{T_{PWM}} \quad (6)$$

Where (t_{on}) the duration of the high state of is the PWM signal, (T_{PWM}) is the total period of the PWM signal (i.e., $T_{PWM} = \frac{1}{F_{osc}}$).

The duty cycle D of a particular PWM controller is also dependent on the voltage at the control input and the reference voltage V_{ref} . The feedback network and reference voltage are frequently in charge of controlling the relationship. If ($V_{control}$) is the voltage at the control input, the duty cycle can be approximated by (7).

$$D = \left(\frac{V_{control} - V_{min}}{V_{max} - V_{min}} \right) \quad (7)$$

Where ($V_{control}$) is the voltage applied to the PWM control input, (V_{min}) and (V_{mix}) are the minimum and maximum voltages corresponding to 0% and 100% duty cycle, respectively. Practically, in this circuit, the oscillation frequency could be adjusted via the potentiometer resistor R5, as shown in Figure 2.

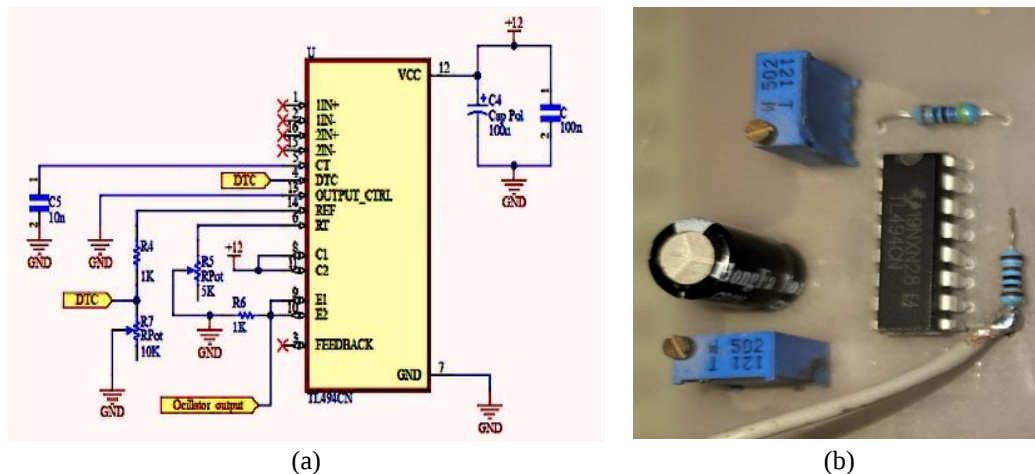


Figure 2. PWM controller circuit: (a) schematic circuit design and (b) PCB design

TL494 has the properties of strong anti-interference ability, basic structure, high fidelity, and low cost. The schematic circuit and PCB circuit of the TL494 as an oscillator are shown in Figure 3. Pin 13 is connected to the ground to benefit from the operation and disconnection of transistors at the same time. The dead-time comparator has a 120-mV input offset, which limits the minimum output dead-time to around 4% of the saw tooth wave period and the maximum duty cycle. Dead-time is the time when there is no overlap and a lower chance of short circuits since both output transistors are off. The voltage given to the dead-time control pin (pin 4) determines the dead-time by (8).

$$D_{\text{dead}} = \frac{V_{\text{DT}} - 0.7\text{V}}{3.3\text{V}} \quad (8)$$

Where V_{DT} is the voltage at the dead-time control pin (pin 4). The dead-time can be adjusted by varying V_{DT} .

The minimum dead-time occurs when V_{DT} is 0.7 V, and the maximum dead-time occurs when V_{DT} equals 3.3 V. This parameter is critical in avoiding cross-conduction in the power transistors. In a loop that regulates feedback, the output voltage V_{out} is compared to a reference voltage V_{ref} , and the difference is magnified and utilized to modify the PWM signal's duty cycle. The closed-loop transfer function can be used to analyze the regulatory loop by (9).

$$T(S) = \frac{G(S)}{1+G(S).H(S)} \quad (9)$$

Where $T(s)$ is the closed-loop transfer function, $G(s)$ is the open-loop transfer function of the PWM controller, $H(s)$ is the transfer function of the feedback network.

Pin 9 and pin 10 are outputs to work side by side, but the voltage value is changed alternately from positive to zero. Pin 12 is the supply pin that can be connected to 12 VDC. Pin 14 is connected to a variable resistance. By changing the value of the resistance, time is controlled, and thus the duty cycle is controlled. The output of this circuit is connected to the input of the gate driver circuit.

2.1.3. Gate driver circuit

The gate driver is operated via the pulses that are produced by the PWM controller; accordingly, the IRF640 MOSFET's gate is driven by the TLP250, and the rate at which the gate capacitance is charged or discharged determines how rapidly the MOSFET turns on and off. When the TLP250 outputs a high signal, it charges the gate capacitance C_{gs} through the gate resistor R_{g} . The charging process can be approximated by an RC charging circuit. The gate charge has an impact on how long it takes the MOSFET to turn on or off, R_{G} , and the gate drive current. By (10) and (11), respectively.

$$V_{\text{g}}(t) = V_{\text{CC}} 1 - e^{-\left(\frac{1}{R_{\text{g}} \cdot C_{\text{gs}}}\right)} \quad (10)$$

$$t_{\text{on/off}} = \frac{Q_{\text{G}}}{I_{\text{G}}} = \frac{Q_{\text{G}} \cdot R_{\text{G}}}{V_{\text{cc}}} \quad (11)$$

Where $V_{\text{g}}(t)$ the gate voltage is at time t , (V_{CC}) is the supply voltage for the TLP250, typically, (R_{g}) is the gate resistor, (C_{gs}) is the gate-source capacitance of the IRF640. The gate charging time constant (T) is provided by (12).

$$T = R_{\text{G}} C_{\text{gs}} \quad (12)$$

As illustrated in Figure 3, the main element in the circuit is the optocoupler (TLP250), which is an optical transistor that has four terminals: the anode, the cathode, the collector, and the emitter. The optocoupler contains a phototransistor that is controlled by giving a light signal to the base terminal to connect or disconnect the current between the collector and the emitter. The most important thing that distinguishes this component is its ability to connect and disconnect within a very short time, estimated at milliseconds. The function of this element in the circuit is to operate and disconnect the MOSFET very quickly and correctly, and to give it the appropriate current. The gate drive current I_{G} is supplied by the TLP250 during turn-on and turn-off transitions. This current determines how fast the MOSFET can switch on or off (13).

$$I_{\text{G}} = \frac{V_{\text{CC}}}{R_{\text{G}}} \quad (13)$$

TLP250 is suitable for gate-driving circuits of power MOSFETs. The supply current is 11 mA, the output current is ± 2 A, the switching time is 0.5 μs , and the isolation voltage is 2500 Vrms. Capacitors of 100 μF and 4.7 μF were used at the output of TLP250. The capacitor at the output of TLP250 was used for protection. The gate driver circuit is shown in Figure 4. The power MOSFET IRF640 was used for switching purposes; it works either in the cutting zone or the saturation zone. The gate charge (Q_{G}) and driving current (I_{G}) determine the switching times by (14) and (15), respectively.

$$t_{\text{on}} = \frac{Q_{\text{g(on)}}}{I_{\text{G}}} \quad (14)$$

$$t_{\text{off}} = \frac{Q_{\text{g(off)}}}{I_{\text{G}}} \quad (15)$$

Where $Q_{g(on)}$ is the gate charge required to turn the MOSFET on, where $Q_{g(off)}$ is the gate charge required to turn the MOSFET off. The VCC range for TLP250 is 10-35 V. Here, an R3 resistor was used across the gate and source to prevent accidental turn-on of the MOSFET by external noise. Hence, a resistance of typically $100\ \Omega$ was used for gate protection. Capacitors C1 and C2 provide a constant voltage (12 V) on the IC, reducing noise. Furthermore, the whole practical design circuit, including the boost converter, PWM controller, and switching circuit, is depicted in Figure 4. To show the different waveforms at the different circuit stages, an oscilloscope (UTD 2025CL, 25 MHz, 250 MS/s) was used.

The power supply model (MODEL: Gpc-3020) was used to offer DC power, which would be inverted into AC. The power supply was set to offer 12 VDC to feed the boost converter circuit, i.e., the output of the power supply is an input for the boost converter circuit. The output of the boost converter circuit is represented by the VCC terminal, which is connected to the switching circuit at the drain terminal of the MOSFET. The PWM controller circuit is connected to the terminal VCC (pins 8 and 11 in IC TL494) for biasing by 12 VDC. The output of the PWM controller circuit was connected to pins 9 and 10. In the switching circuit, the input of this circuit is the output of the oscillator circuit that is connected to the resistance R1 on pin 2 of the main element in the optocoupler circuit (TLP250), and pin 8 is the input of the driver circuit that is fed with a value of 12 VDC.

2.1.4. Considerations for closed-loop voltage regulation

While this study focuses on characterizing the open-loop performance to establish baseline efficiency, the chosen TL494 controller is inherently equipped for closed-loop regulation [28]. A feedback loop can be implemented by sensing the output voltage via a resistive divider and feeding it back to one of the TL494's internal error amplifiers (pin 3). The amplifier would then compare this feedback signal to the internal 5 V reference, automatically adjusting the PWM duty cycle (D) to maintain a constant output voltage under varying load conditions or input fluctuations. Implementing such a control loop would be a straightforward extension to enhance the inverter's practical robustness, and its stability could be analyzed using standard control theory methods to ensure a fast transient response without overshoot.

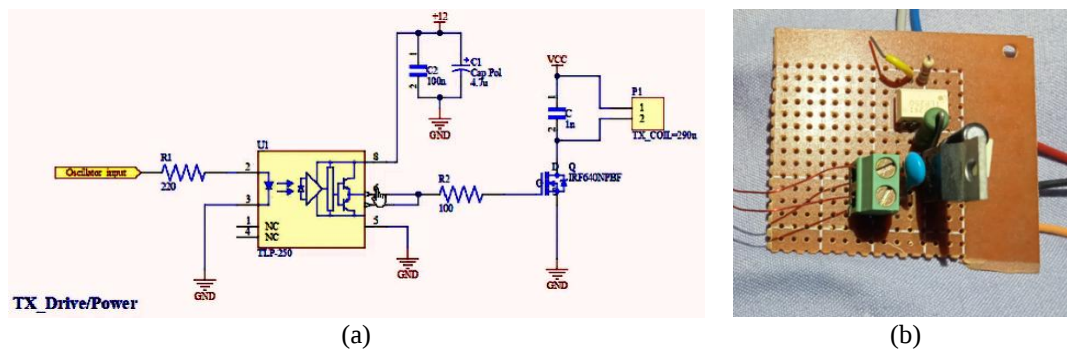


Figure 3. MOSFET with gate driver circuit: (a) schematic circuit and (b) practical circuit

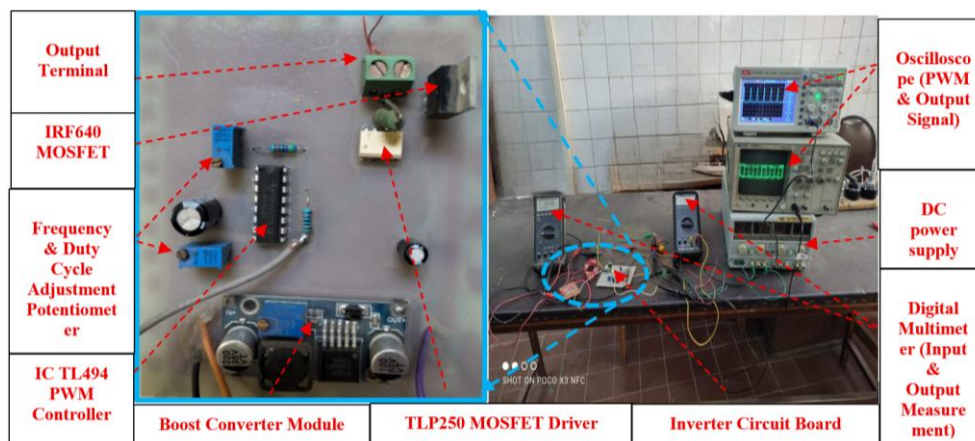


Figure 4. The designed inverter and experimental setup

3. RESULT AND DISCUSSION

For the simulation side, results showed that the optimal recorded efficiency was 98% when the frequency was sweeping between 40 kHz and 110 kHz; this optimal efficiency was obtained at 70 kHz when the load was fixed at 100 Ω . Furthermore, results showed that the optimal recorded efficiency was 84.7% when the load was sweeping between 50 Ω and 1000 Ω ; this optimal efficiency was obtained at 50 Ω when the frequency was fixed at 100 kHz. Figure 5 shows the waveform of the generated pulses that were obtained by the developed PWM controller circuit with an amplitude of 10.2 V at a frequency of 91.27 kHz. Furthermore, Figure 6 shows the output waveform of the inverter circuit via the MOSFET switch terminal, which had a peak voltage of 20 V.

From an experimental perspective, the maximum efficiency achieved during a frequency sweep (40–110 kHz) was 96.96% at 55 kHz, compared to a minimum of 51.25% at 110 kHz with a 100 Ω load. Similarly, the system was tested by sweeping the load from 50 Ω to 1000 Ω at a fixed frequency of 100 kHz. Under this condition, the maximum achieved efficiency was 80% at 50 Ω , whereas the minimum efficiency declined to 37% at a load of 1000 Ω .

Further analysis of the output waveform in Figure 6 revealed a peak-to-peak voltage ripple of approximately 0.8 V on the DC input to the switching stage, which is considered acceptable. A Fourier analysis of the simulated output waveform was performed in LTspice, yielding a Total Harmonic Distortion (THD) of approximately 48%. While this value is inherent to a square wave, it is suitable for WPT applications where the receiver coil is typically part of a resonant circuit that naturally filters out higher-order harmonics, effectively delivering a sinusoidal current to the load.

Figure 7(a) shows the simulation and experimental efficiency results of the proposed designed inverter at a load resistance of 100 Ω when the frequency was sweeping from 40 kHz to 110 kHz. Moreover, the simulation and experimental output voltage results are shown in Figure 7(b). It can be seen that the voltage losses increase with increasing frequency; however, these losses are still acceptable. Figure 8 shows the efficiency vs. the change in the load resistance value from 50 Ω to 1000 Ω when the frequency was fixed at 100 kHz. From Figures 7 and 8, it can be noticed that both simulation and experimental results are convergent.

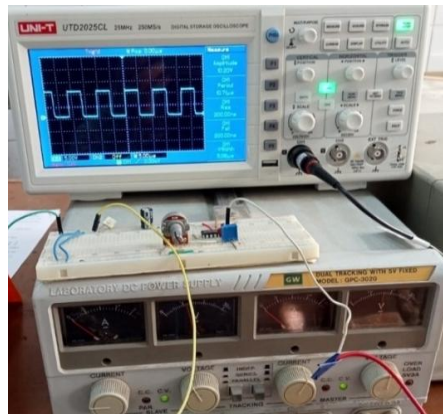


Figure 5. The output voltage waveform of the PWM controller circuit

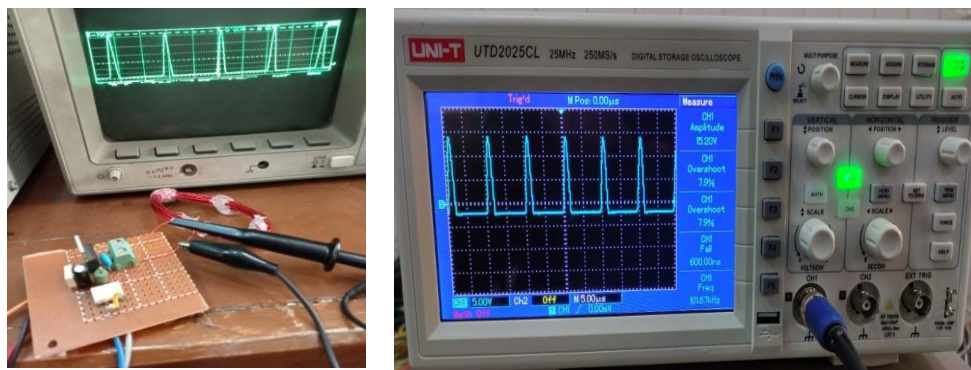


Figure 6. The output voltage waveform of the proposed inverter

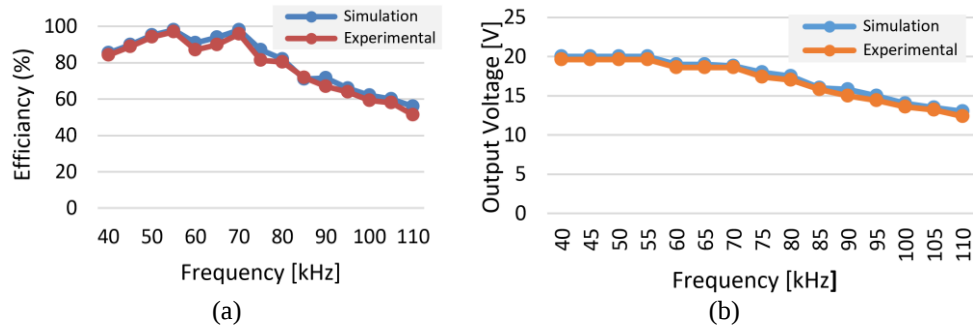


Figure 7. Experimental and simulation results at the fixed load of 100 Ω : (a) efficiency vs. frequency sweeping and (b) output voltages vs. frequency sweeping

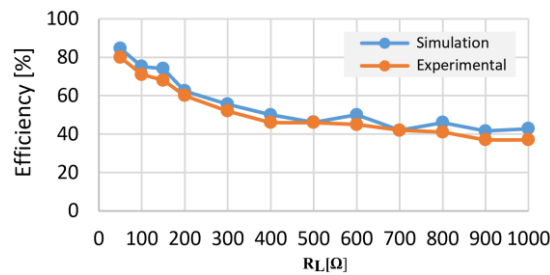


Figure 8. Experimental and simulation results of the efficiency versus change in load resistance value at a fixed frequency of 100 kHz

However, when the frequency is increased, efficiency decreases, showing that the recorded efficiency at the higher frequency of 110 kHz was 56% recorded by simulations and 51.25% recorded by experiments. However, the efficiency at the higher frequency of 110 kHz is still acceptable. To take advantage of the advantages of high frequencies for WPT applications, which permit more accurate and efficient energy transfer, as well as possibly lowering interference and permitting fewer receiver and transmitter components. Therefore, using the suggested design more frequently is preferred. The most important feature of this design is that the total cost is low for designing a high-frequency inverter using a single MOSFET at 110 kHz for the WPT application, which avoids circuit complexity and reduces the value of losses since this design requires fewer components compared to other designs of inverters. The highest efficiency of the inverter will be calculated in case of a change in frequency value, at a frequency of 55 kHz and a constant load resistance of 100 Ω , using the maximum input and maximum output power. This formula will be used to determine efficiency using (16).

$$\text{Efficiency (EFF)} = \frac{P_{\text{output}}}{P_{\text{input}}} \times 100\% \quad (16)$$

Given input current = 0.33 A and the input voltage = 12 volts.

$$P_{\text{in}} = V_{\text{in}} \times I_{\text{in}} \quad (17)$$

$$P_{\text{in}} = 12 \times 0.33 = 3.96 \text{ W} \quad (18)$$

Given output voltage = 19.6 Volts and load resistance = 100 Ω .

$$P_{\text{out}} = \frac{V^2}{R_L} = \frac{(19.6^2)}{(100)} = 3.84 \text{ W} \quad (19)$$

Through (17) and (19), the highest value of the output efficiency was calculated.

$$\text{Efficiency (EFF)} = \frac{3.84}{3.96} \times 100\% = 96.96\% \quad (20)$$

The highest inverter efficiency will be calculated if the load impedance value changes at a resistor of 50 Ω , and the frequency is fixed at 100 kHz using maximum input and maximum output power. This formula will be used to determine efficiency using (21).

$$\text{Efficiency (EFF)} = \frac{7.22}{8.92} \times 100\% = 80\% \quad (21)$$

Table 1 shows detailed experimental results of the literature for different load conditions, frequency, and efficiency compared with the proposed work.

Table 1. An analysis of the proposed work in relation to the literature

Reference	Frequency	V_{out}	Efficiency [%]	Load [Ω]
[29]	100 kHz	24 V	86.4% at 52.4 Ω	52.4 Ω to 220 Ω
[30]	592 kHz	-	71.3% at 5 Ω , 66.4% at 100 Ω	5 Ω to 100 Ω
[31]	13.56 MHz	-	95.4%	21.8 Ω
[32]	13.56 MHz	-	96.1%	50 Ω
Proposed work	40 kHz: 110 kHz	19 V	96.96% at 55 kHz at fixed load 100 Ω 80% at 50 Ω at fixed frequency	50 Ω to 1000 Ω

Thermal and reliability analysis: To ensure the reliability of the inverter under continuous operation, a thermal analysis was conducted on the critical power component. The analysis focused on the IRF640 power MOSFET, as it is the component subjected to the highest thermal stress in the system. Consequently, the total power dissipation (P_{Total}) in the MOSFET is calculated as the sum of conduction losses (P_{cond}) and switching losses (P_{sw}). Conduction loss occurs when the MOSFET is in its 'ON' state and is calculated using (22).

$$P_{cond} = I_{D(RMS)}^2 \times R_{DS(on)} \quad (22)$$

Where: $I_{D(RMS)}$ is the root mean square (RMS) value of the drain current; $R_{DS(on)}$ is the drain-to-source on-resistance of the MOSFET, which is approximately 0.18 Ω according to the component datasheet.

Switching loss occurs during the brief turn-on and turn-off transitions and is generally proportional to the operating frequency. The junction temperature (T_j), which is the internal temperature of the semiconductor die, is a critical indicator of reliability. It can be estimated using (23).

$$T_j = T_A + P_{Total} \times R_{\theta JA} \quad (23)$$

Where: T_A is the ambient temperature, assumed to be a standard 25 $^{\circ}\text{C}$ for this analysis; and P_{Total} is the total power dissipated by the MOSFET (in Watts).

The parameter $R_{\theta JA}$ represents the junction-to-ambient thermal resistance of the device. This value quantifies how effectively heat is transferred from the semiconductor junction to the surrounding ambient air. For the IRF640 MOSFET in a standard TO-220 package without an external heatsink, this resistance is approximately 62 $^{\circ}\text{C}/\text{W}$ as specified in the manufacturer's datasheet.

Based on the experimental measurements under the highest stress condition tested (output power of 7.22 W at 100 kHz with a 50 Ω load), the total power dissipation (P_{Total}) was estimated to be approximately 0.8 W, accounting for both conduction and estimated switching losses at this frequency [33]. Substituting these values into (24).

$$T_j = 25^{\circ}\text{C} + (0.8\text{W}) \times (62^{\circ}\text{C}/\text{W}) = 25^{\circ}\text{C} + 49.6^{\circ}\text{C} \approx 74.6^{\circ}\text{C} \quad (24)$$

The thermal analysis yielded a calculated junction temperature of approximately 75 $^{\circ}\text{C}$, which remains significantly lower than the IRF640 MOSFET's limit of 150 $^{\circ}\text{C}$. Such a result indicates that the system maintains thermal stability without requiring additional cooling components like external heatsinks. This configuration ultimately supports the design's objectives of being low-cost and compact for practical WPT implementations.

4. CONCLUSION

This paper presents efficient design considerations for high-frequency, low-power inverters that could be used in WPT applications. Experimental results show the effectiveness of the proposed system under different parameters such as load variation and different frequency modulation. Tests showed a good

convergence between simulation and experimental results. The proposed inverter has some features that can be concluded as follows. Low cost and simple design compared to other inverters in literature, the inverter is suitable for low power electronic applications, it works under different loads with acceptable efficiency, the PWM frequency can be controlled as needed, that is, according to the frequency required by the application, a wide range of input voltage can be applied to the inverter (5–20 V) since it is not designed for a specific value, thus obtaining various voltage values at the output (4–30 V). Such positive points make the proposed design suitable for a variety of applications, not just a specific one. Future work can be done on utilizing the proposed inverter in solar energy by making the solar panel input into the inverter and then transmitting the solar energy wirelessly instead of a wired approach. It is acknowledged that the high-frequency, hard-switching nature of this inverter topology is a potential source of electromagnetic interference (EMI). Although quantitative EMI measurements were beyond the scope of this study, standard mitigation techniques can be applied to ensure compliance with regulatory standards such as ISO 7637. These include implementing a proper ground plane in the PCB layout, adding bypass capacitors close to the ICs, and potentially incorporating a small snubber circuit across the MOSFET to dampen voltage spikes. These simple additions align with the low-cost and minimalist philosophy of the proposed design.

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Kyrillos K. Selim	✓	✓	✓	✓		✓		✓	✓	✓			✓	
Hanem Saied Ebrahim Torad	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
Mostafa R. A. Eltokhy	✓		✓	✓	✓		✓	✓		✓	✓	✓	✓	
Hesham F. A. Hamed		✓	✓		✓	✓	✓		✓		✓	✓		
Mohamed Elzalik		✓	✓	✓		✓	✓	✓	✓	✓			✓	

C : **C**onceptualization

M : **M**ethodology

So : **S**oftware

Va : **V**alidation

Fo : **F**ormal analysis

I : **I**nvestigation

R : **R**esources

D : **D**ata Curation

O : Writing - **O**riginal Draft

E : Writing - Review & **E**ditng

Vi : **V**isualization

Su : **S**upervision

P : **P**roject administration

Fu : **F**unding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article [and/or its supplementary materials].

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